The Abdus Salam
International Centre
for Theoretical Physics

All Programmable SoC based on FPGA for IoT

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- The MLAB was created in 1985 as a joint venture between ICTP and INFN with the aim of having a laboratory for training, research and development open to scientists from developing countries.
- R&D of scientific instrumentation, based on modern technologies, for experimental physics and related applications.

"Scientific thought is the common heritage of humankind."

Abdus Salam

ICTP founder Abdus Salam

ICTP MLAB

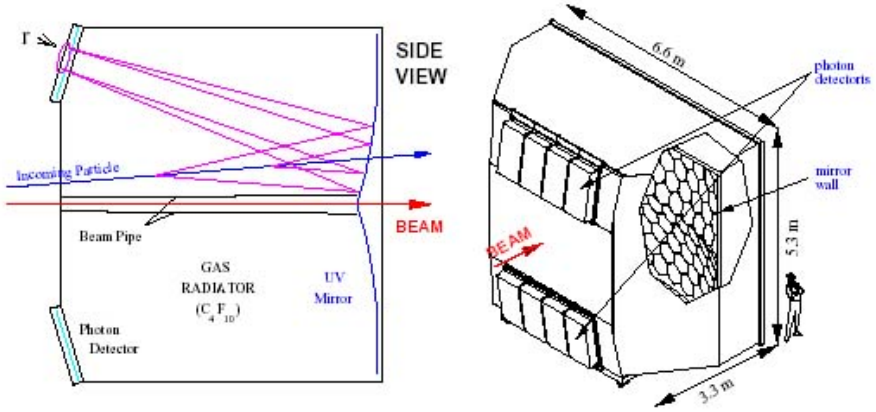
- R&D Collaboration with INFN and other International Institutions

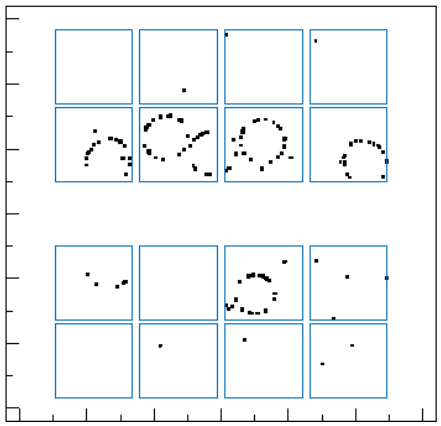
- INFN: innovative multi-channel particle detectors (SDD, MPGD, RICH) and front-end electronics for different applications, including Syncrotron beamlines (Elettra, Trieste) and Particle Physics experiments (CERN, Geneva)

- MLAB:
  - High-performance data acquisition (from ADCs)
  - Real-time data processing (data filtering, digital pulse processing, single photon detection and photon energy measurement, pile-up rejection, measurement of fast electrical discharges, etc)
  - Data transmission to host computer

R&D project

- Data acquisition and processing system for the 83000-chn Cherenkov Photon Detectors of the RICH of COMPASS experiment at CERN
- Data taking since 2004

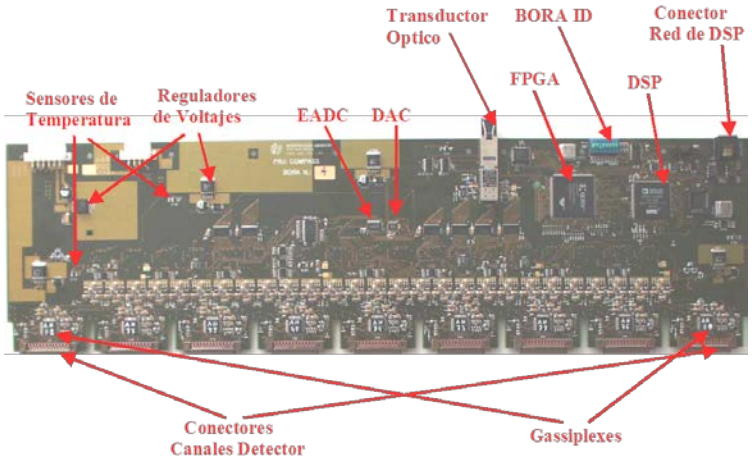




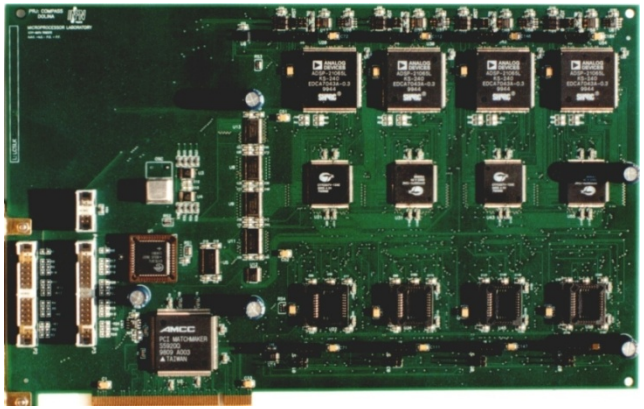
- Challenging specifications:
  - Parallelization and synchronization of sub-systems
  - Reprogrammable and reconfigurable
  - Multi-channel architecture
  - Real-time filtering to reduce the data to be transmitted (programmable thresholds per channel)
  - High-speed dedicated data transmission
  - Remote access and monitoring (**IoT**)
  - Slow control (temperatures, voltages, thresholds , raw data)
  - Synchronization with external signals (trigger, start-of-run, end-of-run, start-of-spill, end-of spill)

FPGA-DSP based system on board

FPGA-DSP board (Bora)
for acquisition, processing and transmission
of 432 channels (192 boards)



Multi-DSP PCI board (Dolina)



- Field Programmable Gate Array (FPGA) as co-processor of a Digital Signal Processor (DSP)

- DSP TDM networks (commands, programming, configuration, thresholds, synchronization signals, engineering packets, raw data, etc) (8 net x 24 dsp)

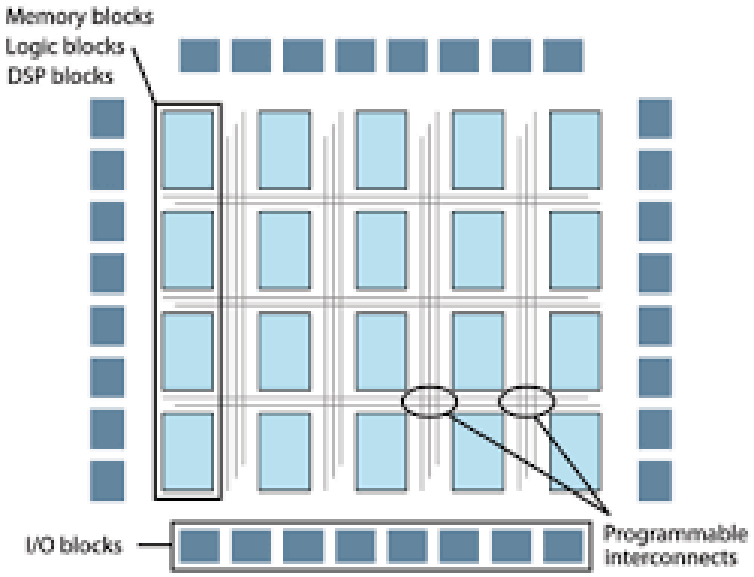
- Operations Modes:
  - Event Mode (FPGA)
    - Peak trigger rate of 800 kHz
    - Acquired data rate up to 80 GB/s
    - Transmitted data rate up to 8 GB/s
  - Channel Characterization Mode

$$T = \mu + \alpha\sigma$$

  - Thresholds Mode
  - Engineering Packets Mode (temp sensors and voltages)
  - Self testing (DAC)

What is an FPGA?

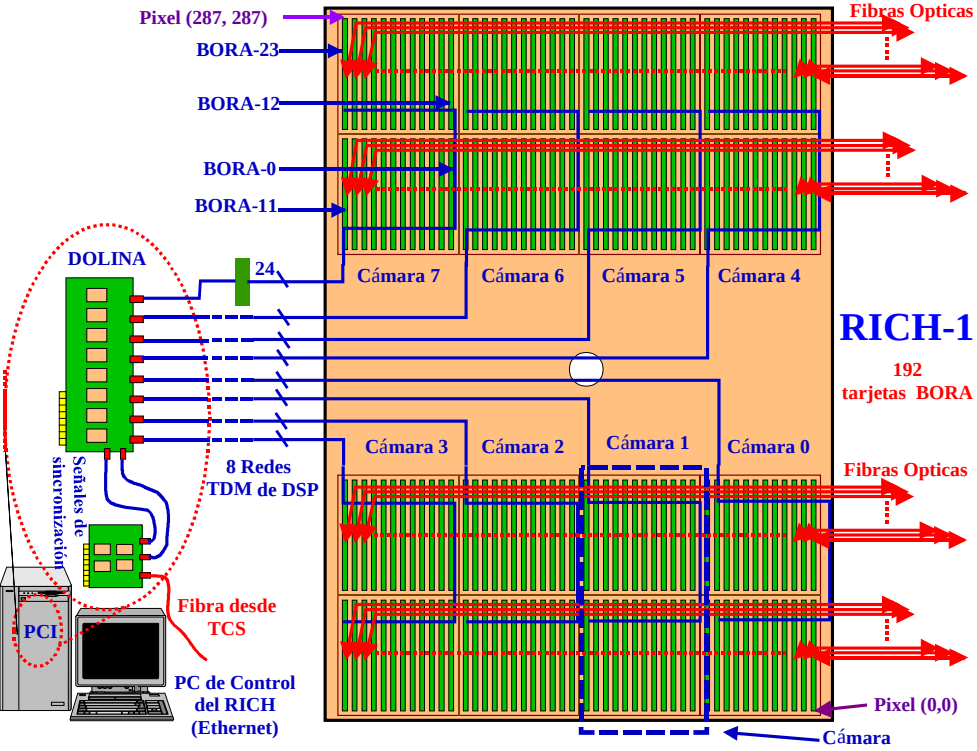
Schematic view

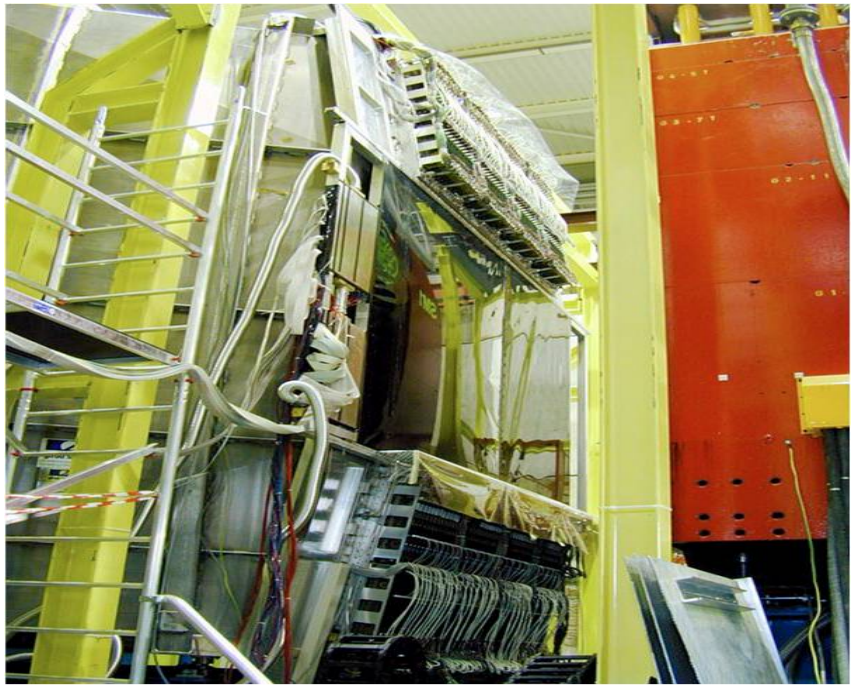


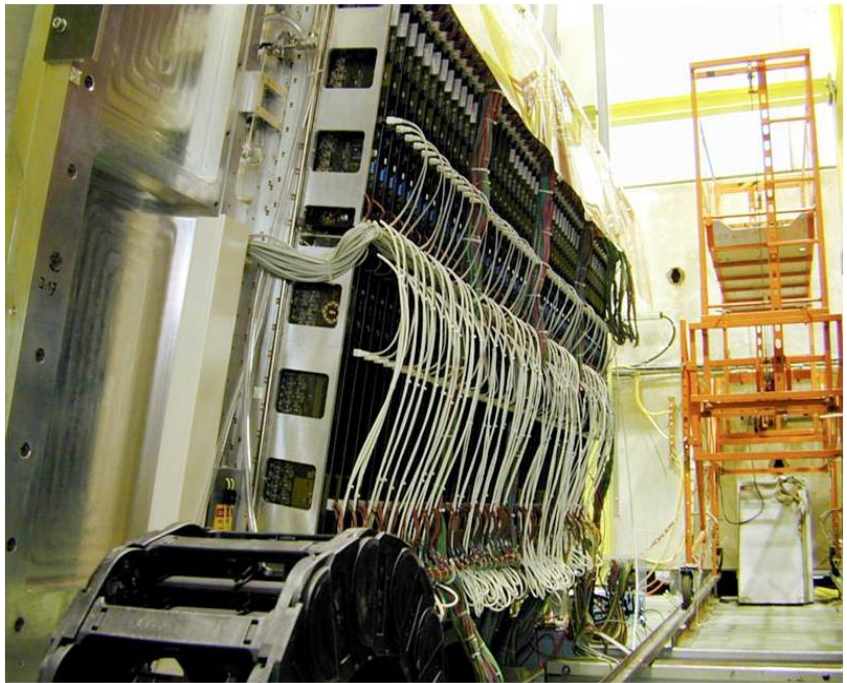
- True dual port RAM
- Clock management units
- Optimized arithmetic blocks (multipliers, DSP)
- Embedded processors (PowerPC)
- Highly specialized In-Out ports (Gbits/sec)

- Field Programmable Gate Arrays are semiconductor devices based on a matrix of configurable logic blocks (CLBs) connected via programmable interconnects.
- A flexible interface
- Some of the most important characteristics are re-configurability, great intrinsic parallelism and high connectivity
- **H**ardware **D**escription **L**anguage (Verilog and VHDL).

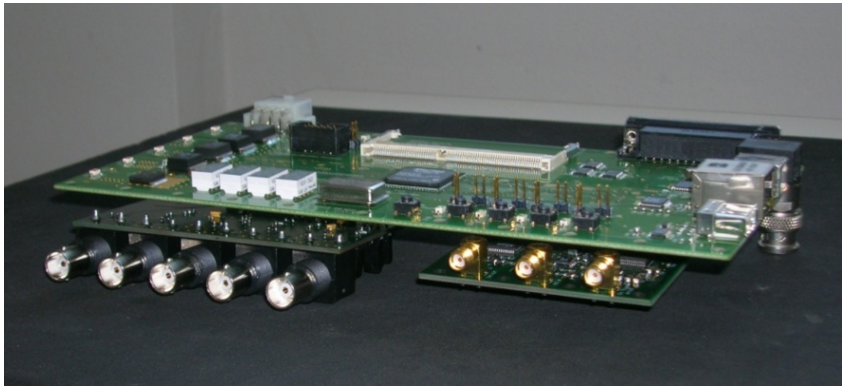
Global Architecture







Hands-On Training Activities



International and Regional Schools and Workshops on DSP and FPGA for Scientific Instrumentation

(Peru 2002, Ghana 2005, Trieste 2006, Colombia 2007, Malaysia 2008, Trieste 2009, Argentina 2010, Mexico 2010, Bangladesh 2011, Cuba 2012, Trieste 2013, Costa Rica 2014, Pakistan 2015)

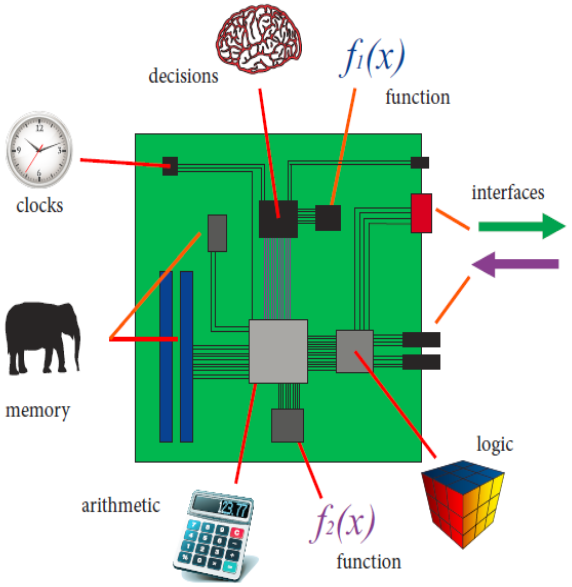
Reconfigurable Virtual Instrumentation board based on FPGA and open source intellectual property

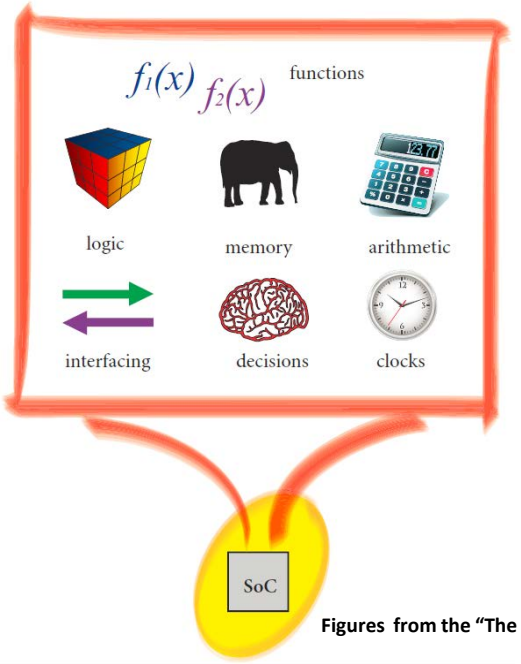
Low-cost reusable hardware/software platform for the emulation of multiple instrumentation systems

- Hardware & Software modularity
- Block-based design methodology
- Common standardized global architecture
- Open Source & Open Hardware

Sharing the design efforts and results among a large community of users and contributors

All Programmable System on Chip (SoC)

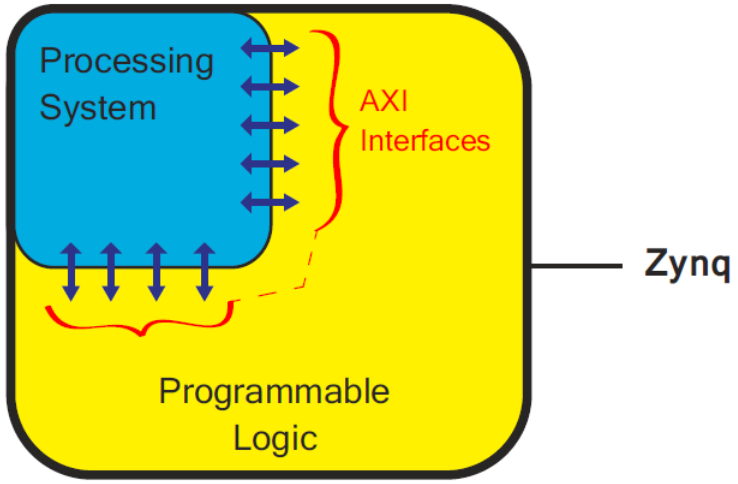


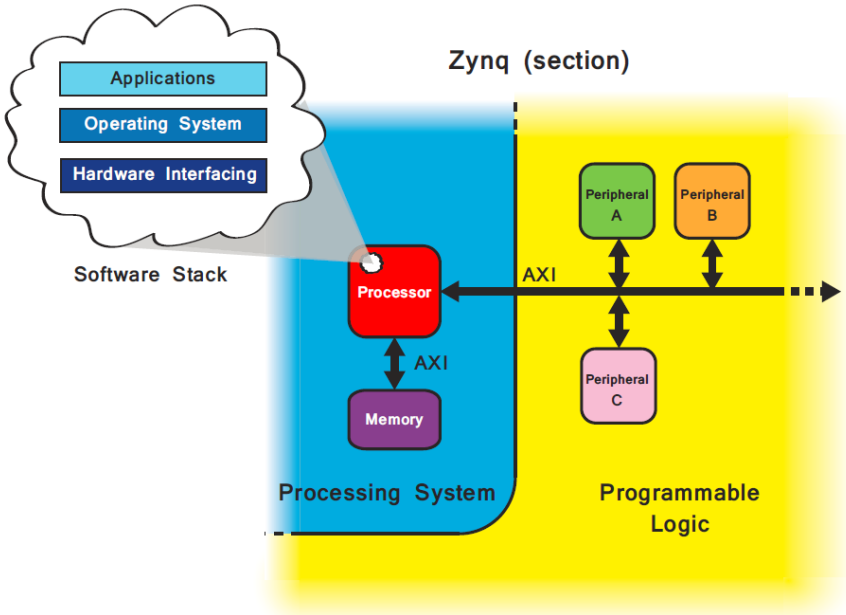


Figures from the "The Zynq Book"

- From Systems on a Board to System on a Chip
- Hybrid devices that combine the software programmability of general purpose processors with the hardware reconfigurability of FPGA in the same physical device.
- The SoC solution is lower cost, enables faster and more secure data transfers, has higher overall system speed, lower power consumption, smaller physical size and better reliability

A Simple View of the Zynq-7000 SoC

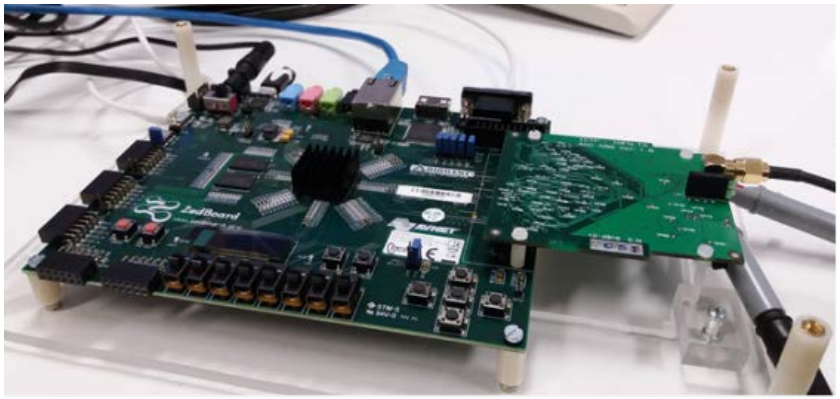




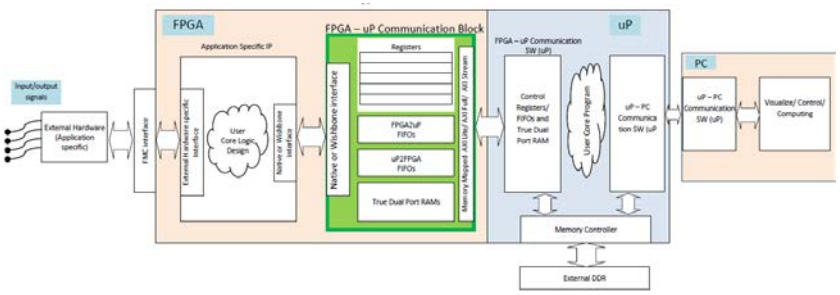
- Integrates FPGA fabric and a dual-core ARM Cortex-A9 processor
- The overall functionality of any designed system can be appropriately partitioned between hardware and software
- Links between the PL and PS are made using standard Advanced eXtensible Interface (AXI) connections.
- New opportunities for **IoT**

Figures from the "The Zynq Book"

Hands-On Training Activities on SoC



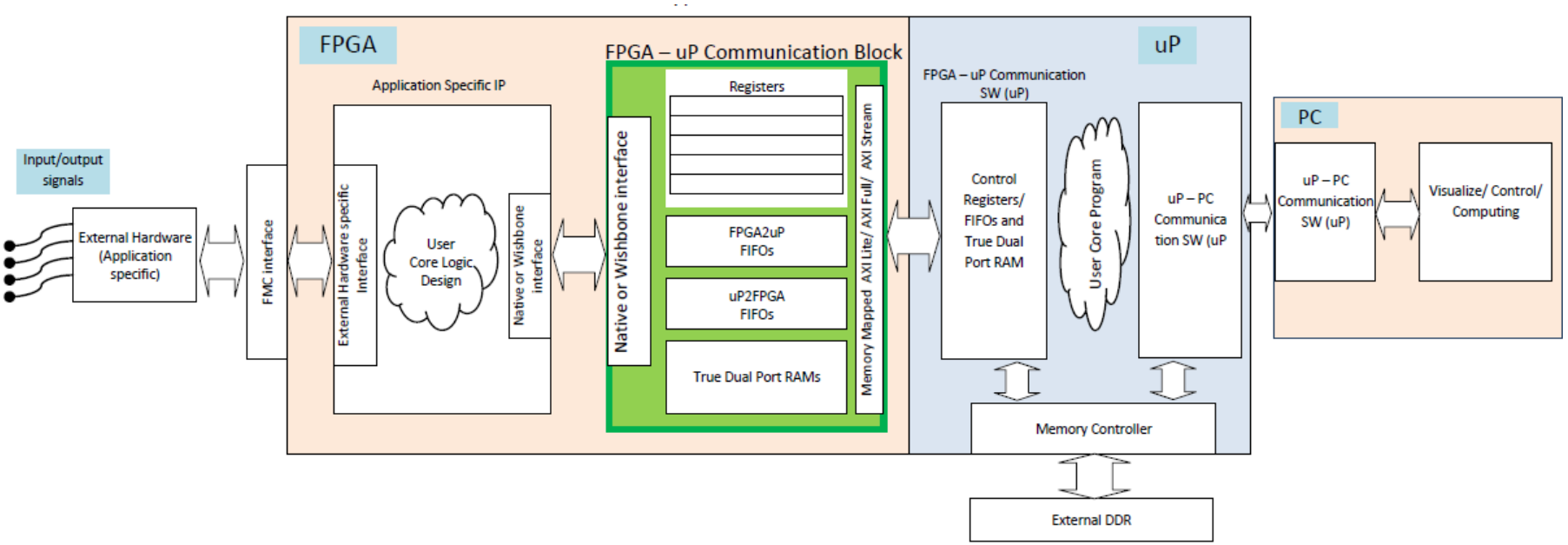
ZedBoard: Zynq Evaluation and Development Board (FMC connector)



- **Training Activities on All Programmable Systems-on-Chip (FPGA+ARM)** for high performance data acquisition, real-time processing, and transmission
- Joint ICTP-IAEA School on Hybrid Reconfigurable Devices for Scientific Instrumentation, ICTP, 2015
- Joint ICTP-IAEA School on Zynq-7000 SoC and its Applications for Nuclear and Related Instrumentation , ICTP, 2017 (four weeks)
- Workshop and Conference on Advanced Reconfigurable Instrumentation for Scientific Applications, Malaysia, 2016
- Advanced Workshop on FPGA-based Systems-On-Chip for Scientific Instrumentation and Reconfigurable Computing , ICTP, 2018

SoC Based Reconfigurable Virtual Instrumentation (RVI)

Typical Global Architecture



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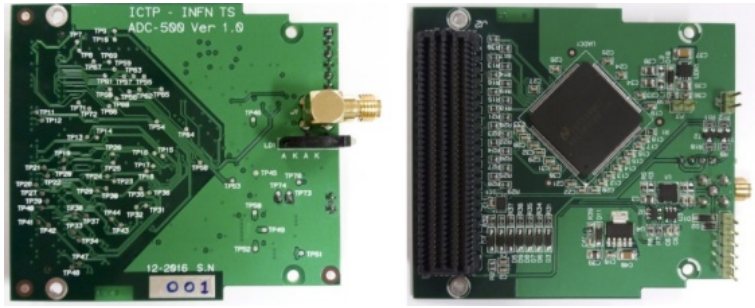
Training and Research Activities based on SoC prototypes

HV systems for Thick-GEM gaseous detectors of single UV photons

- Development a fast FMC data acquisition board (ADC 8-bits 500 MS/s) for high time resolution measurements

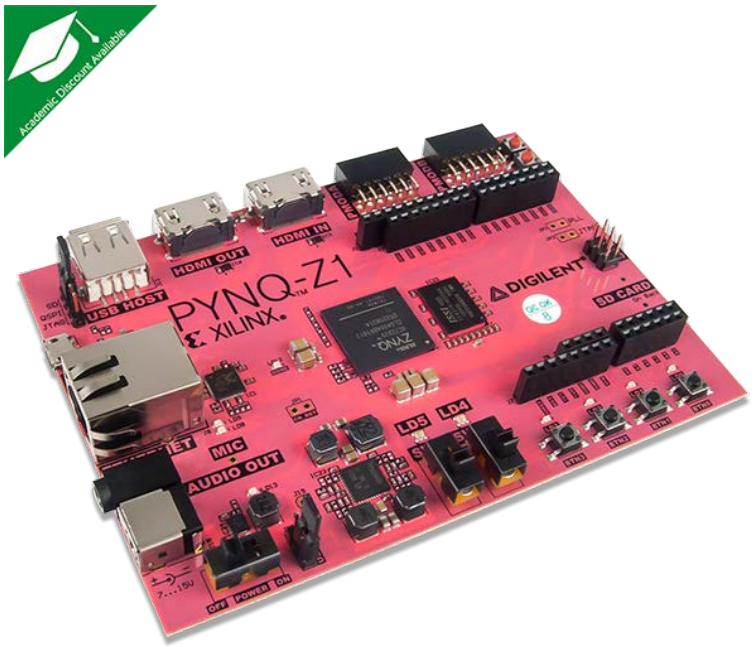


Monolithic 8-channel SDD system

- SDD based system for high-resolution spectroscopy of low-energy x-ray photons (2 kev – 30 kev)
- Development of DPP for on-line single X-ray photon detection and energy measurement at high flux rates (~100000 count/s)
- Characterization at different energies for fluorescence spectroscopy (Elettra and *SESAME synchrotrons)*

PYNQ-Z1 Python Productivity for Zynq-7000

The PYNQ-Z1 board is designed to be used with PYNQ, a new open-source framework that enables embedded programmers to exploit the capabilities of Xilinx Zynq All Programmable SoCs without having to design programmable logic circuits. Instead, the SoC is programmed using Python and the code is developed and tested directly on the PYNQ-Z1. The programmable logic circuits are imported as hardware libraries and programmed through their APIs in essentially the same way that the software libraries are imported and programmed.



DEMO time !